Fig.1

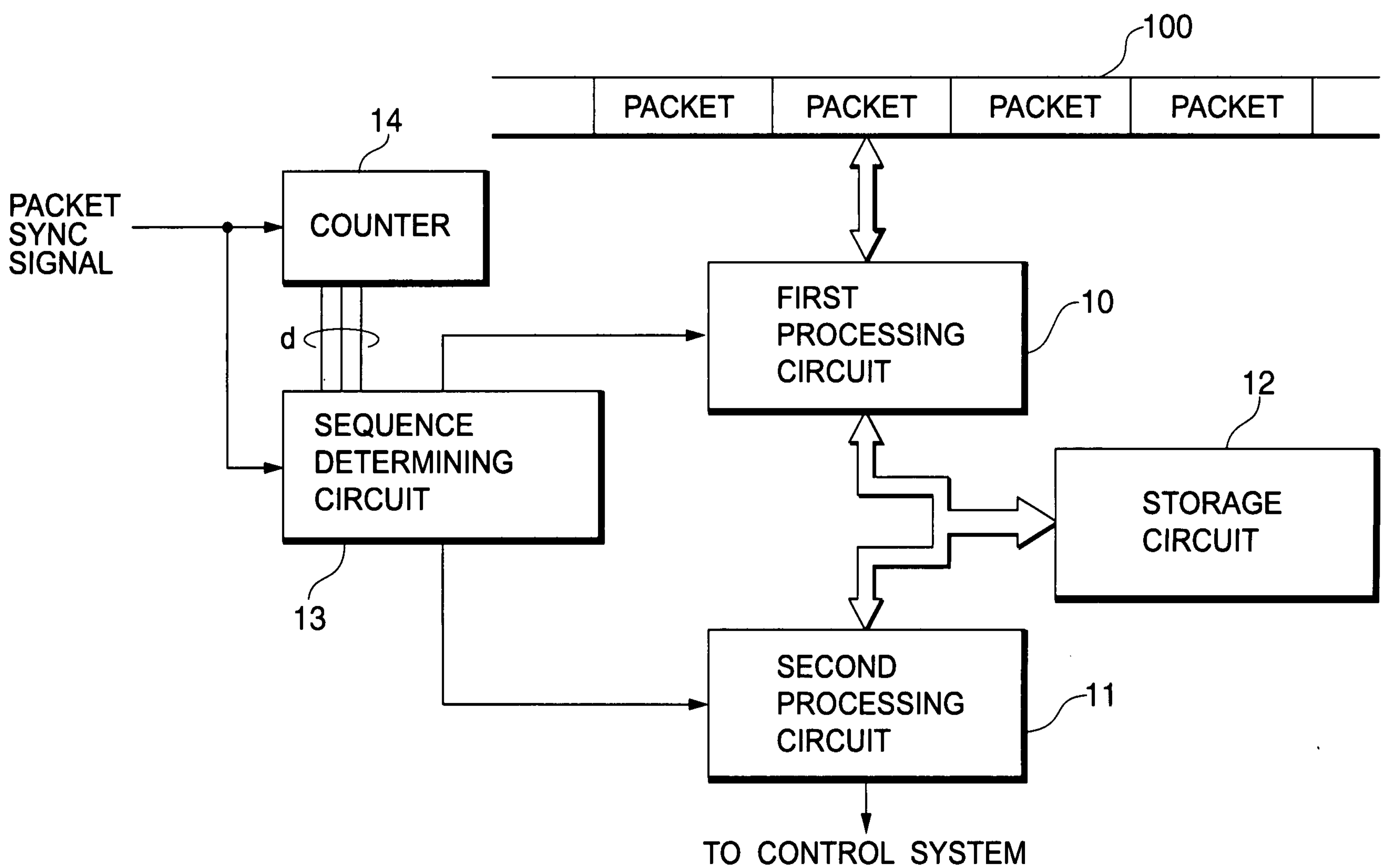

100
PACKET
PACKET
PACKET
PACKET
14
PACKET SYNC SIGNAL
COUNTER
d
SEQUENCE DETERMINING CIRCUIT
13
FIRST PROCESSING CIRCUIT
10
12
STORAGE CIRCUIT
SECOND PROCESSING CIRCUIT
11
TO CONTROL SYSTEM

Fig.2

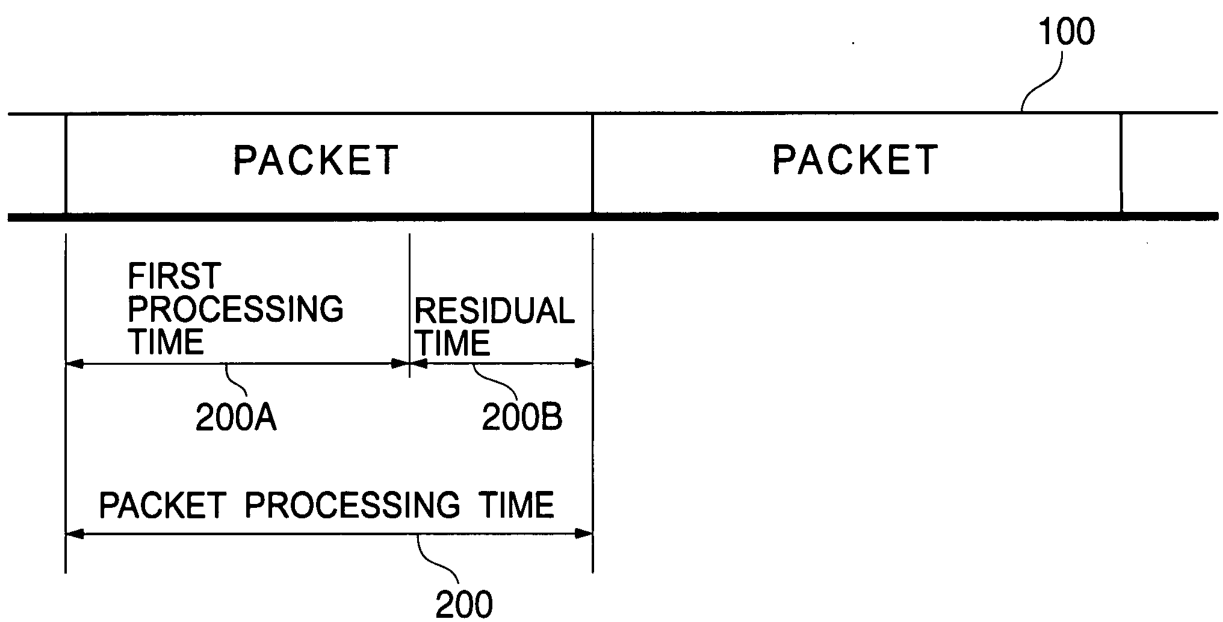

100
PACKET
PACKET
FIRST PROCESSING TIME
RESIDUAL TIME
200A
200B
PACKET PROCESSING TIME
200

Fig.3

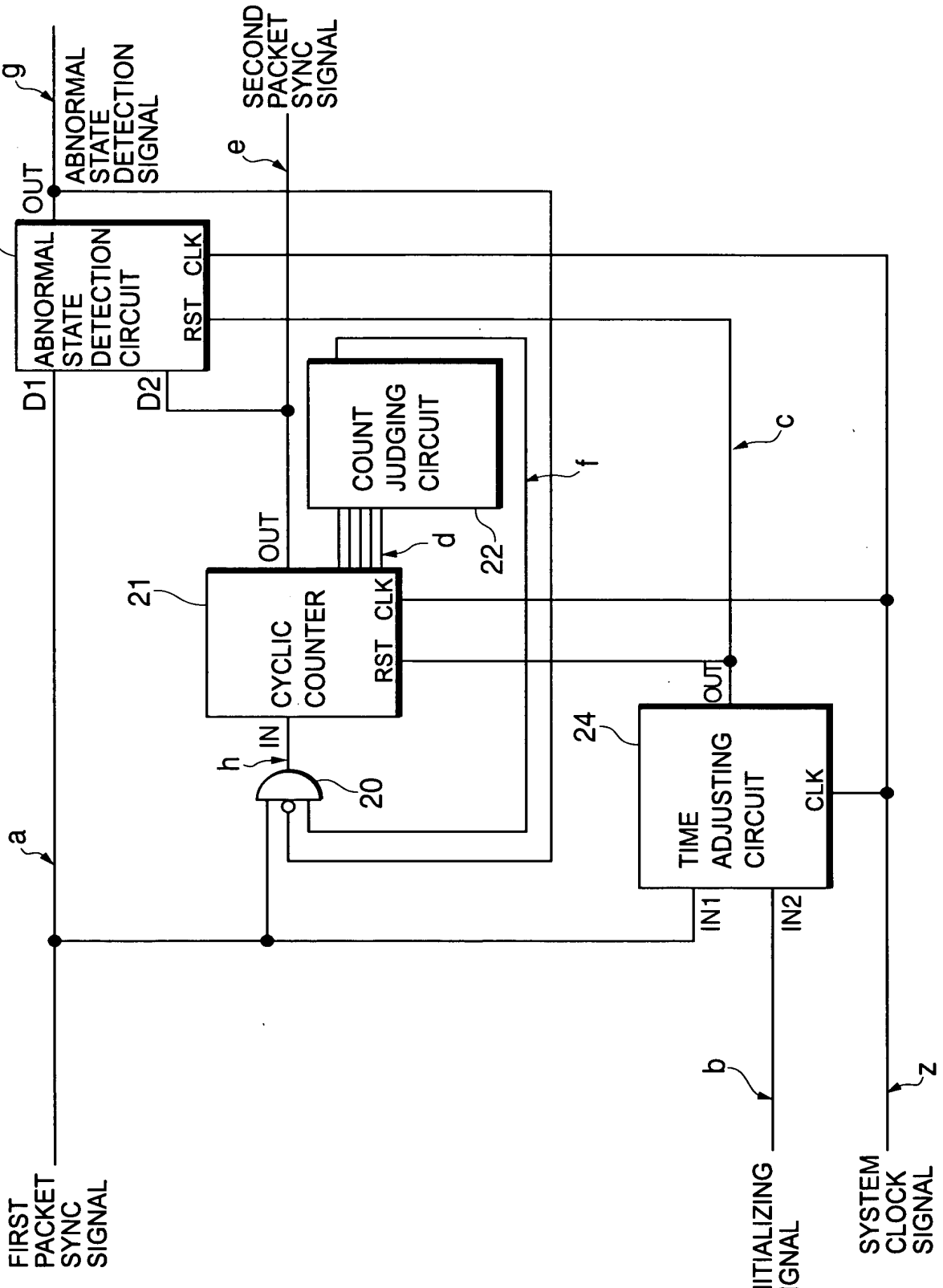

FIRST PACKET SYNC SIGNAL
a
INITIALIZING SIGNAL
b
SYSTEM CLOCK SIGNAL
z
ABNORMAL STATE DETECTION SIGNAL
g
SECOND PACKET SYNC SIGNAL
e
23
ABNORMAL STATE DETECTION CIRCUIT
OUT
RST
CLK
D1
D2
COUNT JUDGING CIRCUIT
22
d
f
c
21
CYCLIC COUNTER
OUT
RST
CLK
h
IN
20
24
TIME ADJUSTING CIRCUIT
OUT
IN1
IN2
CLK

Fig.4

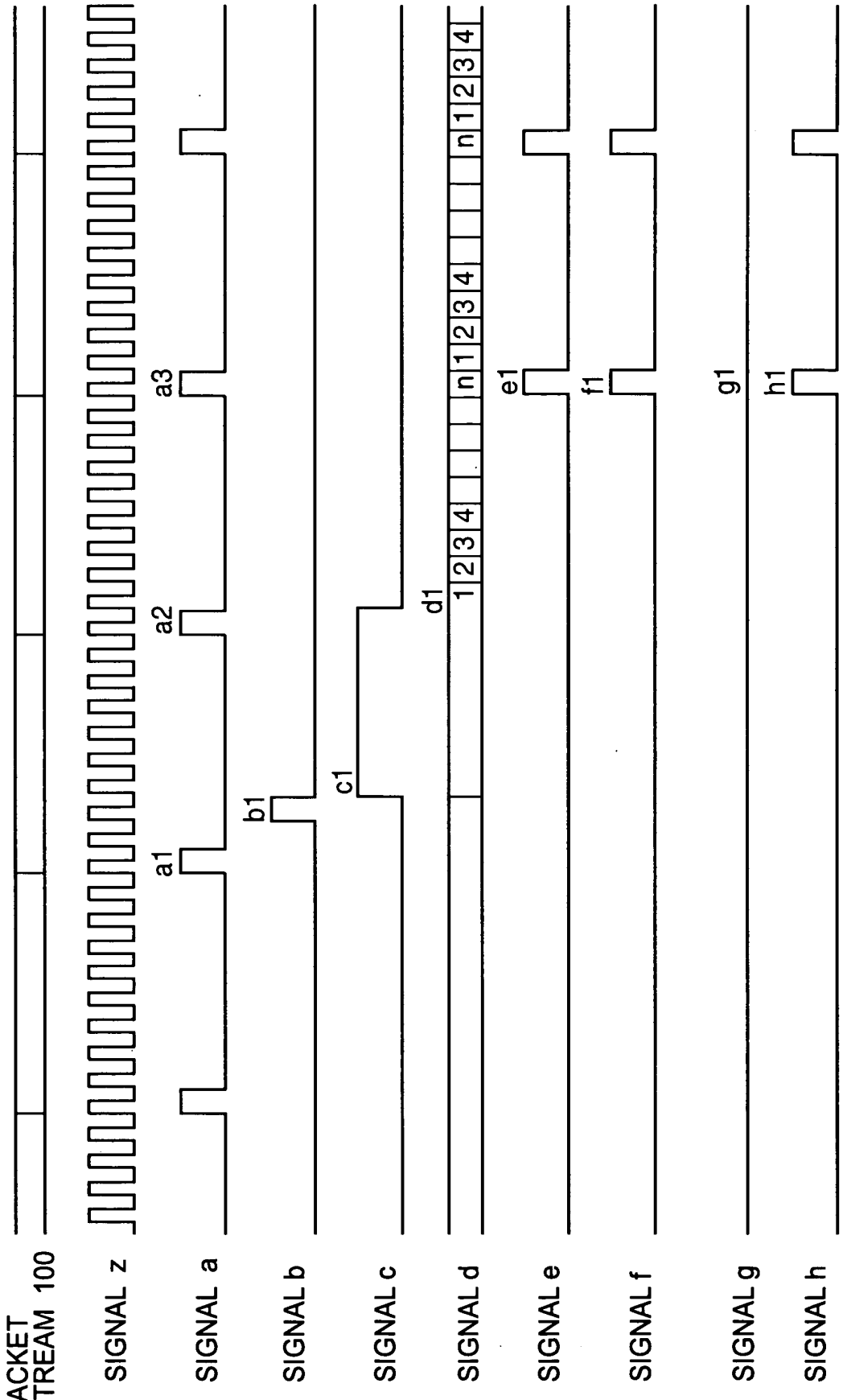

PACKET STREAM 100
SIGNAL z
SIGNAL a
SIGNAL b
SIGNAL c
SIGNAL d
SIGNAL e
SIGNAL f
SIGNAL g
SIGNAL h
a1
a2
a3
b1
c1
d1
1 2 3 4
n 1 2 3 4
n 1 2 3 4
e1
f1
g1
h1

Fig.5

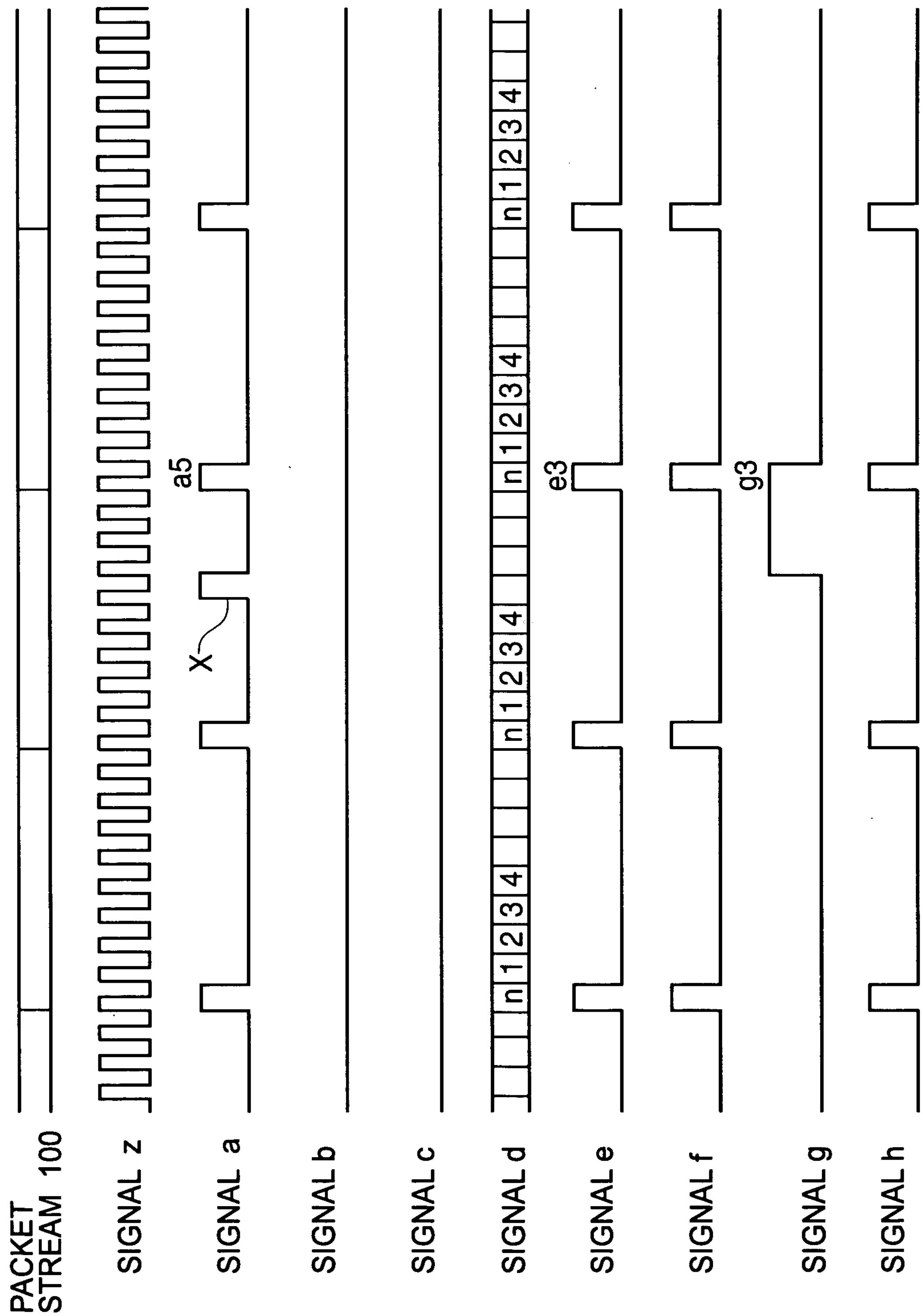

PACKET STREAM 100
SIGNAL z
SIGNAL a
SIGNAL b
SIGNAL c
SIGNAL d
SIGNAL e
SIGNAL f
SIGNAL g
SIGNAL h
a5
X
e3
g3
n 1 2 3 4

Fig.6

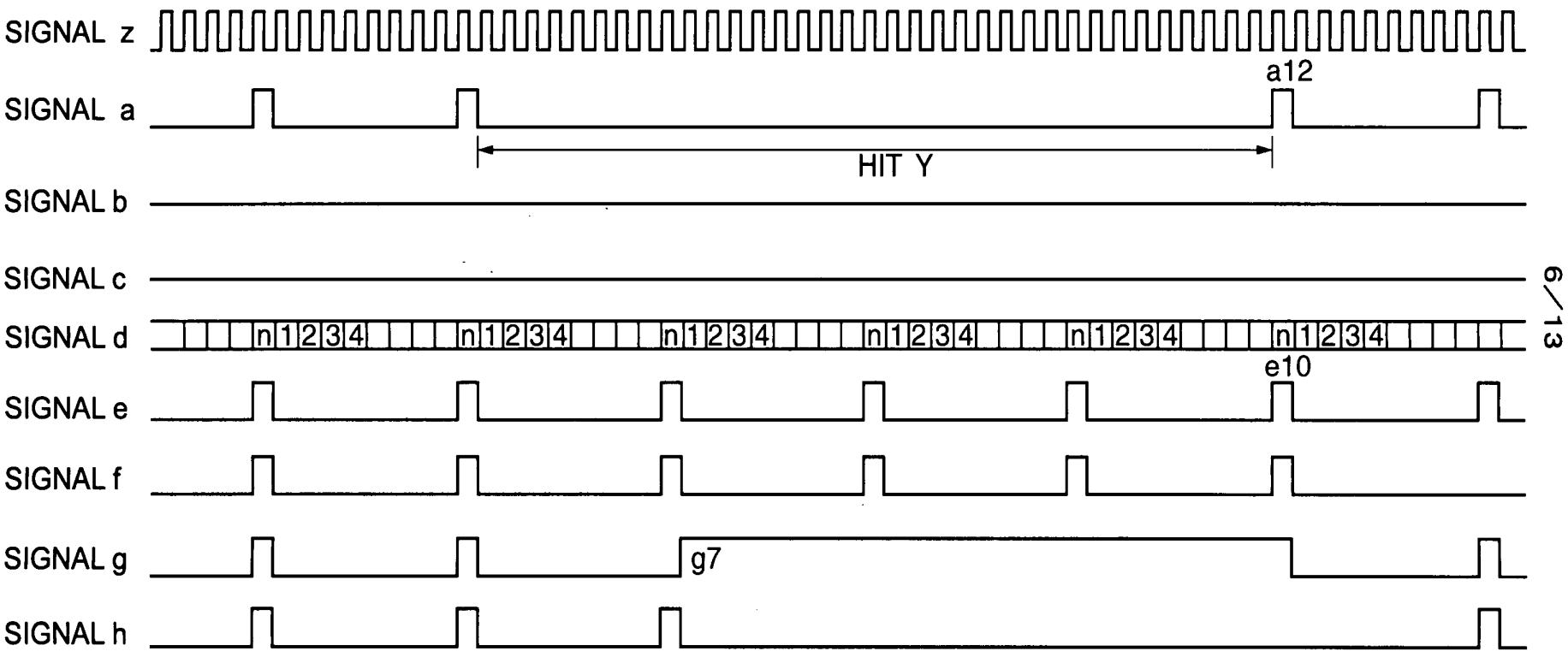

SIGNAL z
SIGNAL a
a12
HIT Y
SIGNAL b
SIGNAL c
SIGNAL d
n1234
e10
SIGNAL e
SIGNAL f
SIGNAL g
g7
SIGNAL h

Fig.7

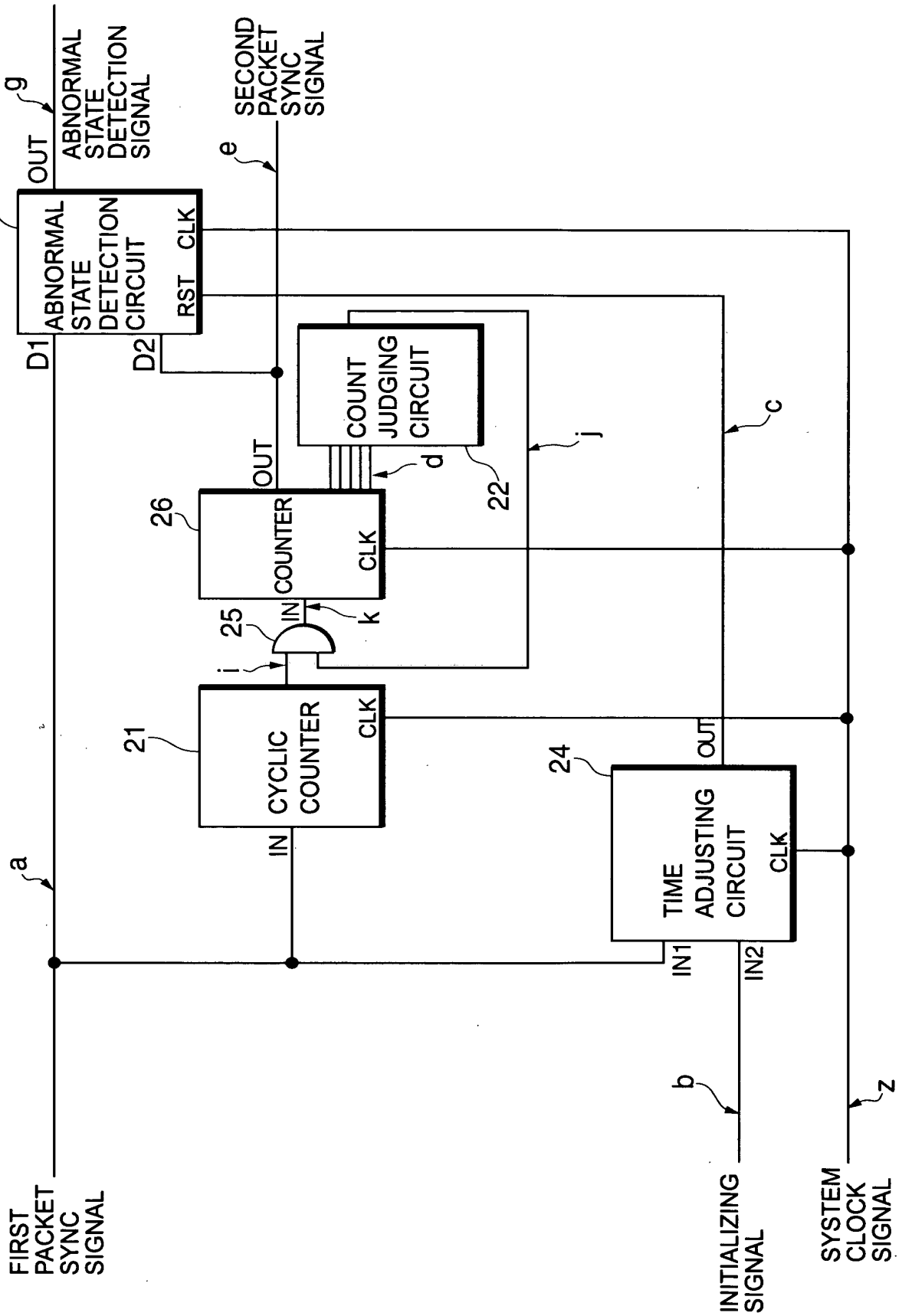

FIRST PACKET SYNC SIGNAL
a
ABNORMAL STATE DETECTION CIRCUIT
23
D1
D2
OUT
RST
CLK
g
ABNORMAL STATE DETECTION SIGNAL
e
SECOND PACKET SYNC SIGNAL
CYCLIC COUNTER
21
IN
CLK
i
25
IN
k
COUNTER
26
OUT
CLK
COUNT JUDGING CIRCUIT
22
d
j
c
TIME ADJUSTING CIRCUIT
24
IN1
IN2
OUT
CLK
b
INITIALIZING SIGNAL
z
SYSTEM CLOCK SIGNAL

Fig.8

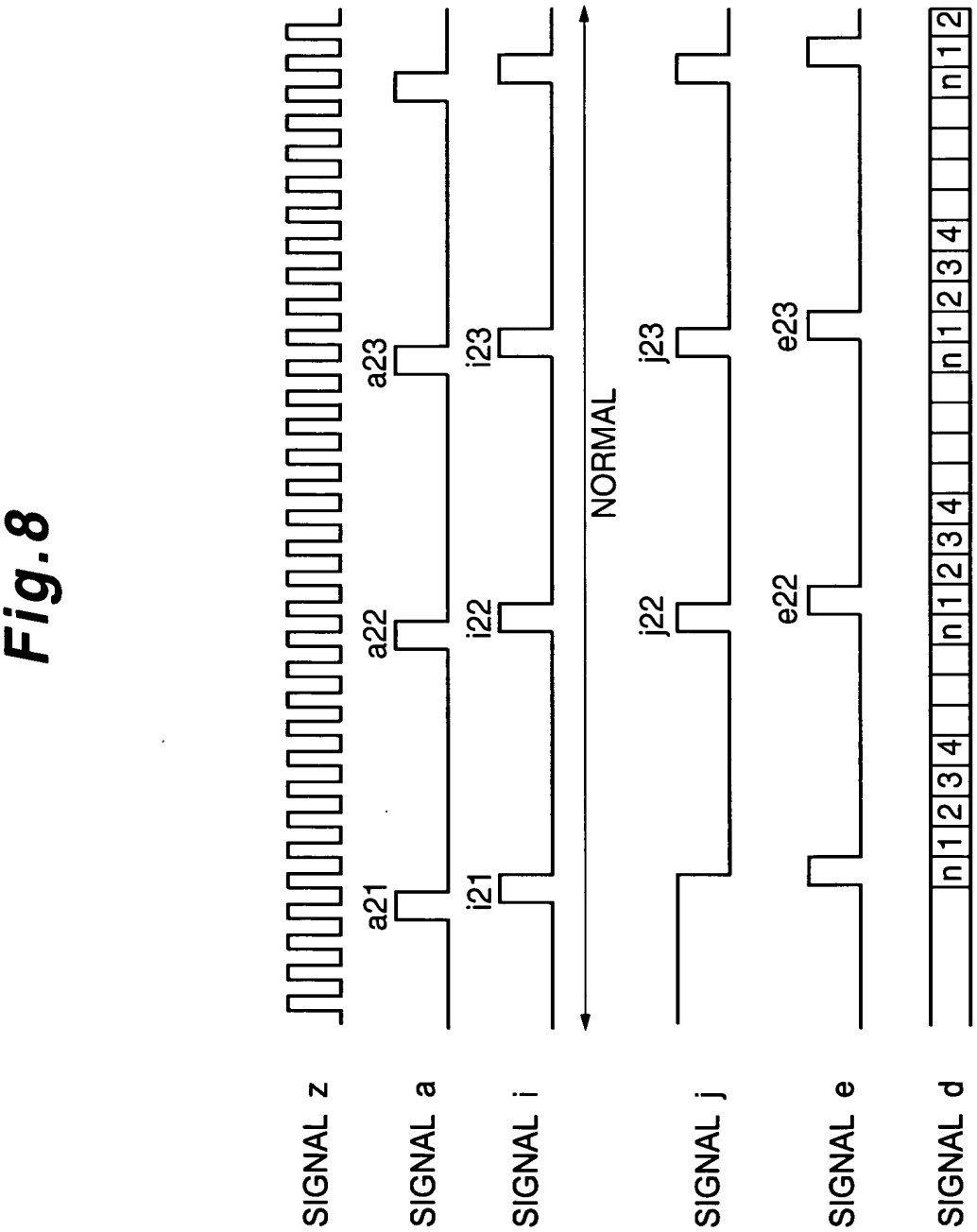

SIGNAL z
SIGNAL a
SIGNAL i
SIGNAL j
SIGNAL e
SIGNAL d
a21
a22
a23
i21
i22
i23
NORMAL
j22
j23
e22
e23
n 1 2 3 4
n 1 2 3 4
n 1 2

Fig.9

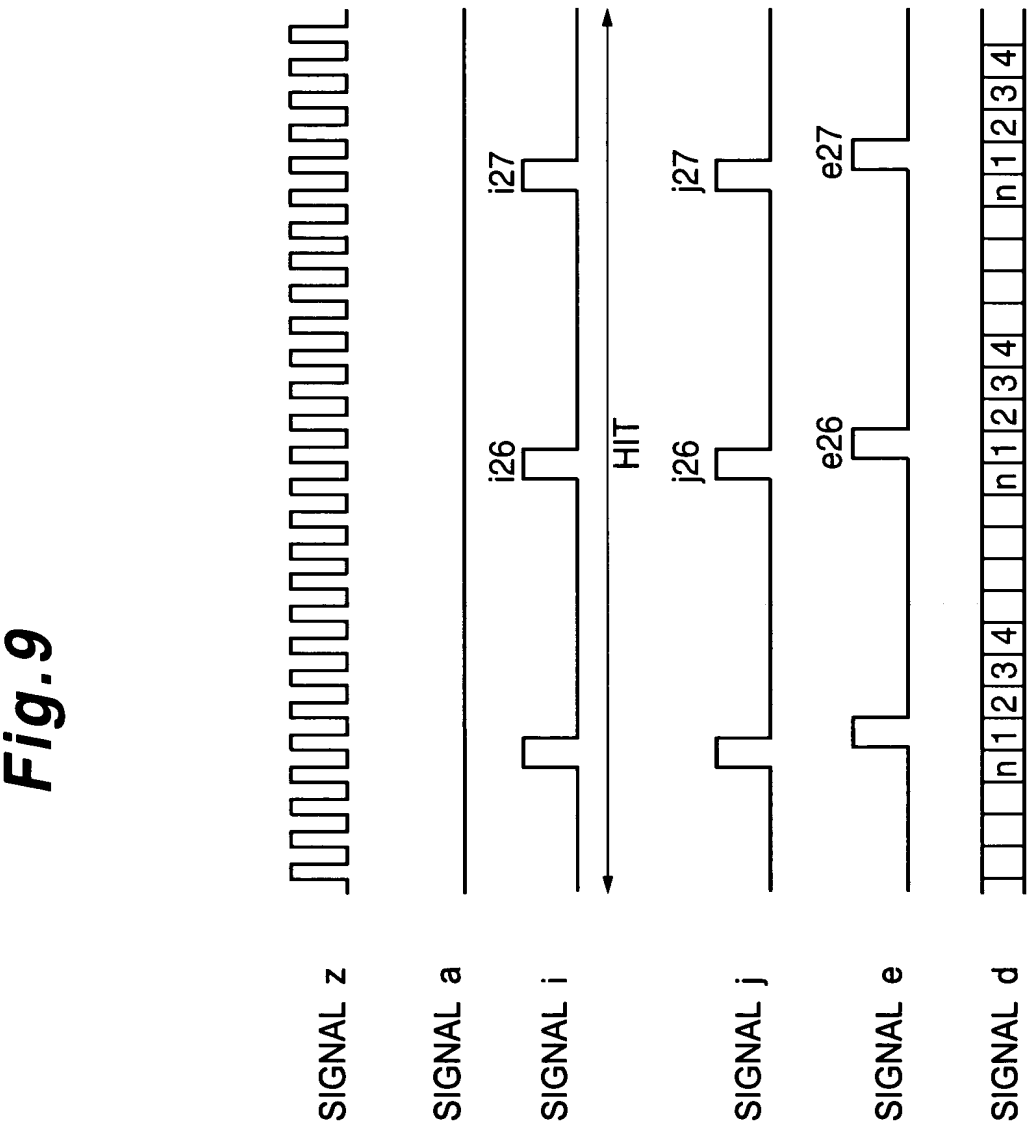

SIGNAL z
SIGNAL a
SIGNAL i
SIGNAL j
SIGNAL e
SIGNAL d
i26
i27
HIT
j26
j27
e26
e27
n 1 2 3 4 n 1 2 3 4 n 1 2 3 4

Fig.10

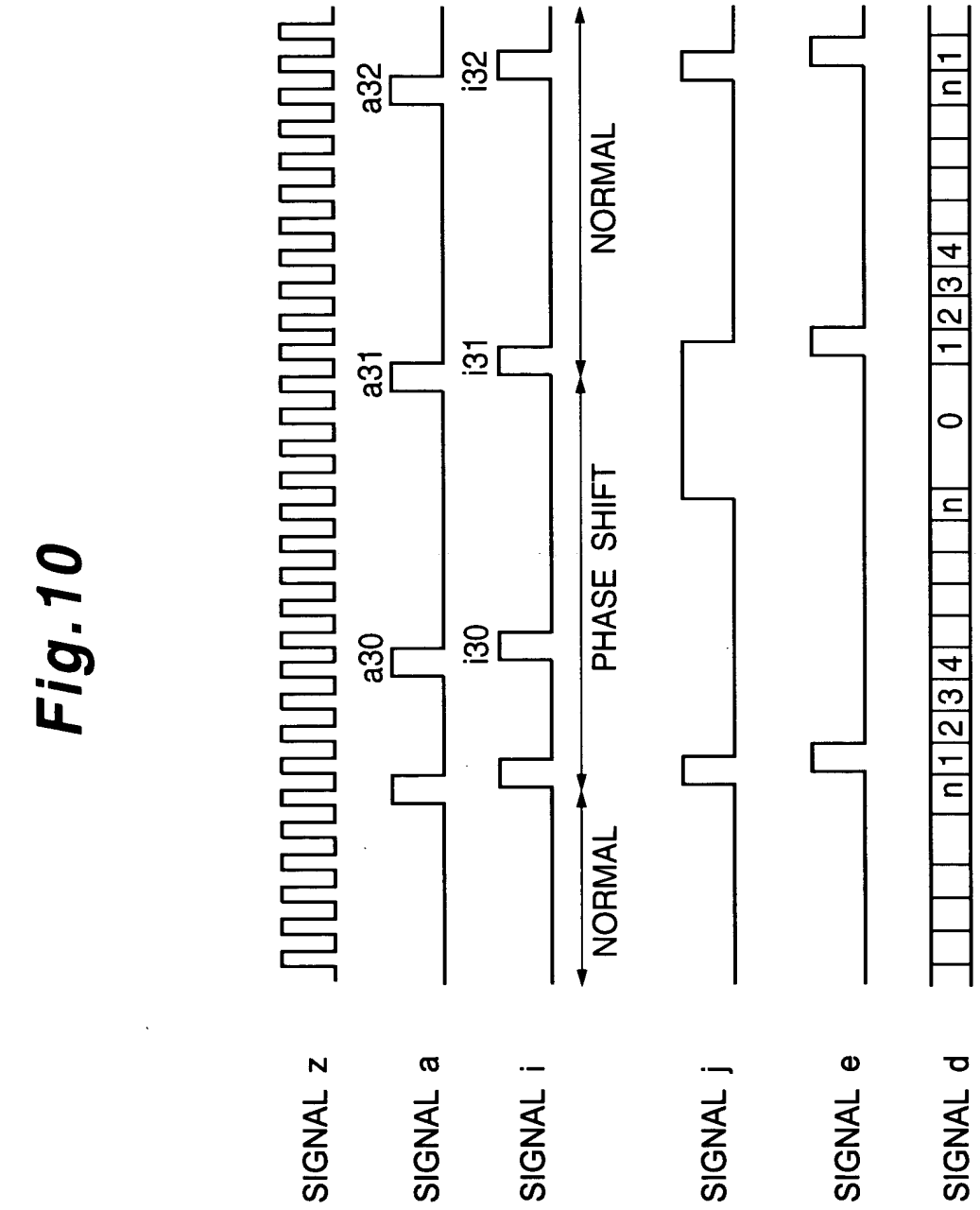

SIGNAL z
SIGNAL a
SIGNAL i
SIGNAL j
SIGNAL e
SIGNAL d
a30
a31
a32
i30
i31
i32
NORMAL
PHASE SHIFT
NORMAL
n 1 2 3 4
n
0
1 2 3 4
n 1

Fig.11

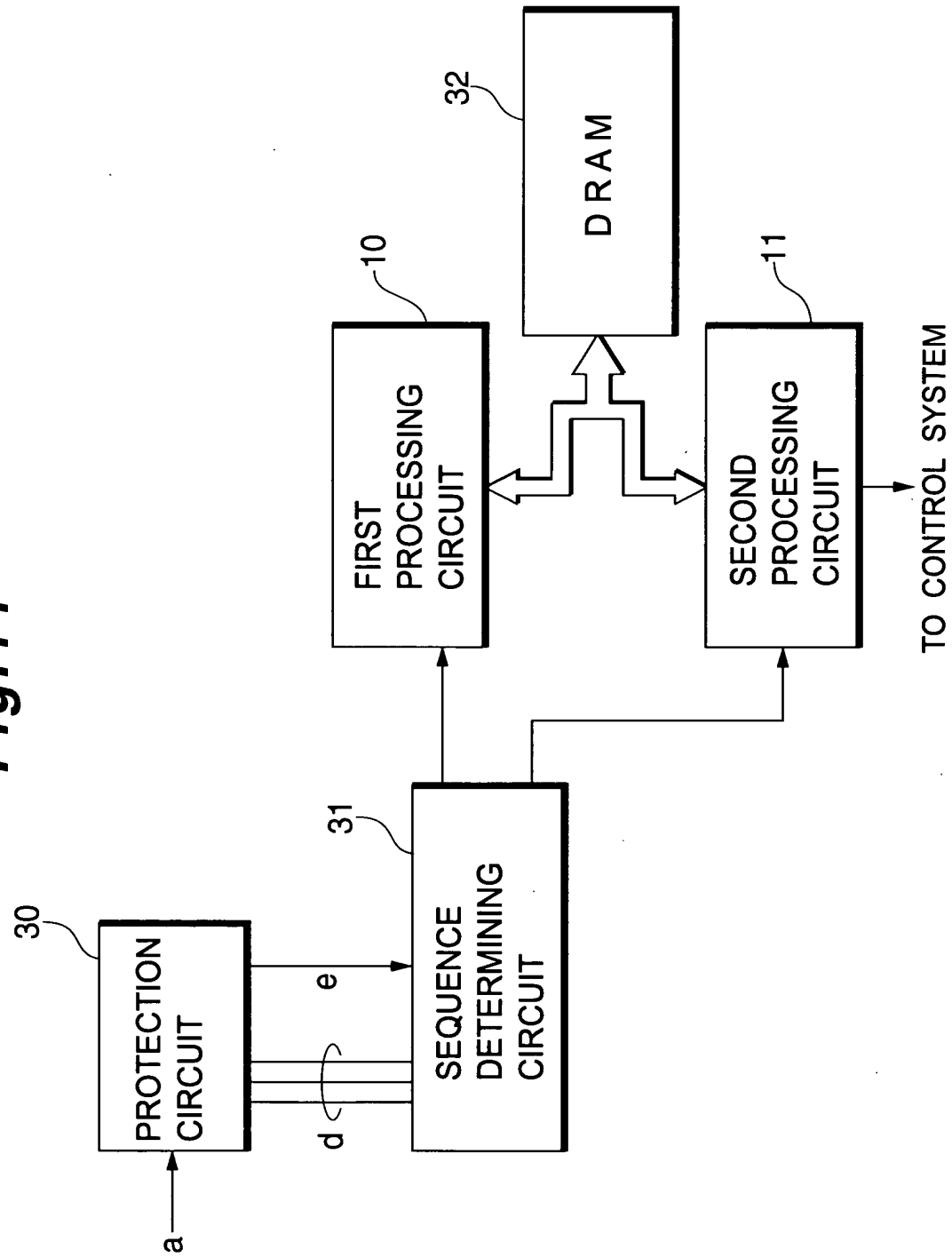

32
DRAM
10
11
FIRST PROCESSING CIRCUIT
SECOND PROCESSING CIRCUIT
TO CONTROL SYSTEM
31
SEQUENCE DETERMINING CIRCUIT
30
PROTECTION CIRCUIT
e
d
a

Fig.12

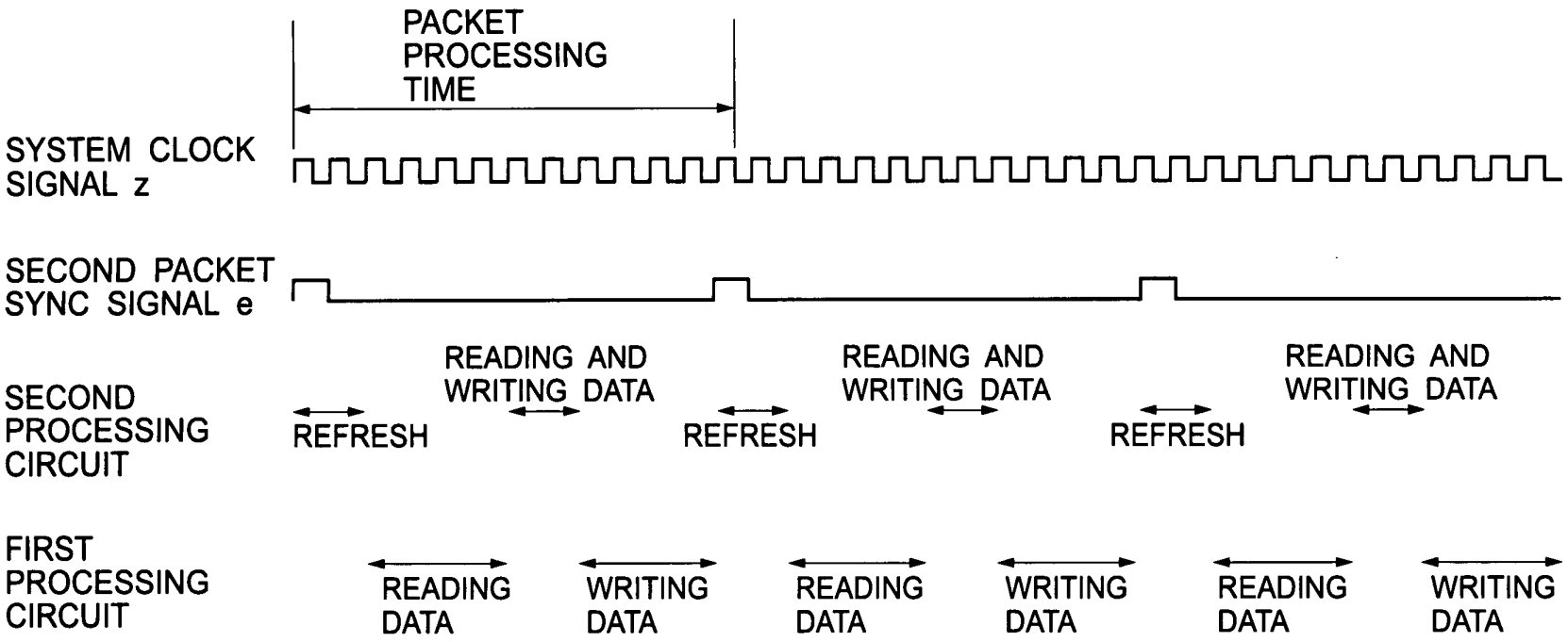
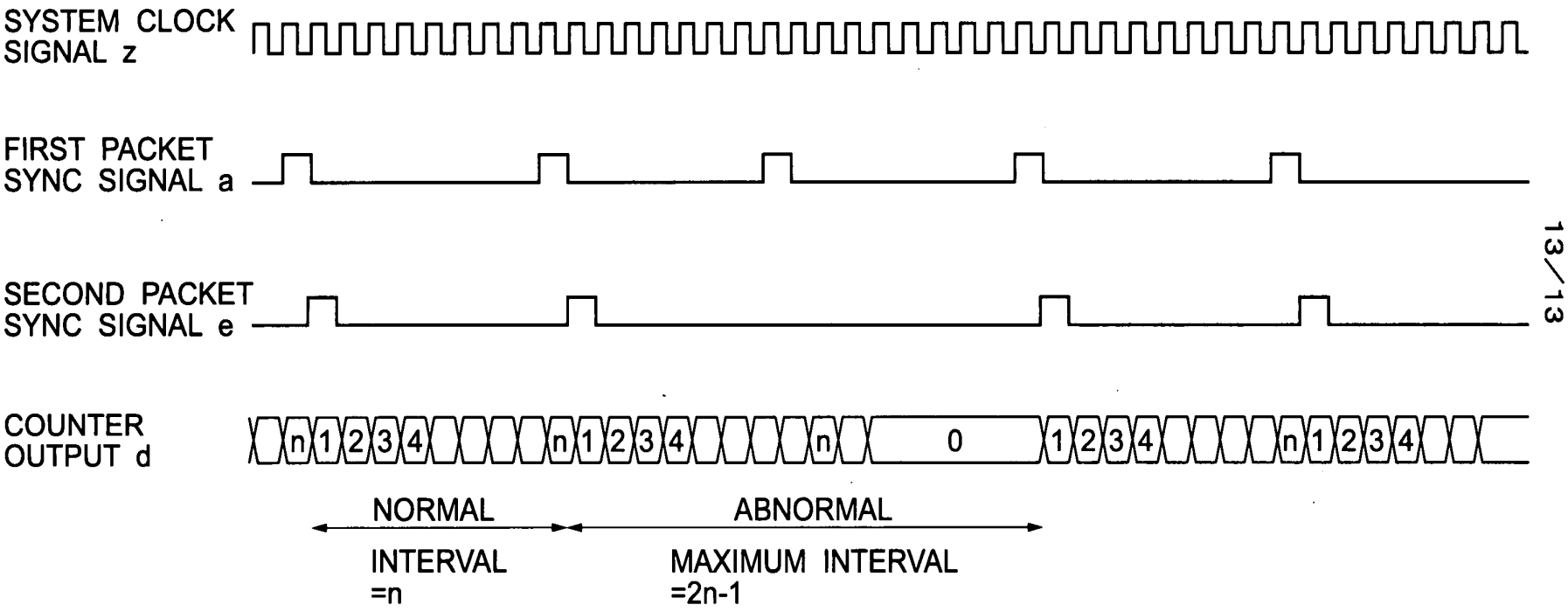

PACKET
PROCESSING
TIME
SYSTEM CLOCK
SIGNAL z
SECOND PACKET
SYNC SIGNAL e
SECOND
PROCESSING
CIRCUIT
READING AND
WRITING DATA
READING AND
WRITING DATA
READING AND
WRITING DATA
REFRESH
REFRESH
REFRESH
FIRST
PROCESSING
CIRCUIT
READING
DATA
WRITING
DATA
READING
DATA
WRITING
DATA
READING
DATA
WRITING
DATA

Fig.13


SYSTEM CLOCK SIGNAL z
FIRST PACKET SYNC SIGNAL a
SECOND PACKET SYNC SIGNAL e
COUNTER OUTPUT d
n 1 2 3 4 n 1 2 3 4 n 0 1 2 3 4 n 1 2 3 4
NORMAL
ABNORMAL
INTERVAL =n
MAXIMUM INTERVAL =2n-1